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AK197B Datasheet

Version：V1.3

Date：2023.03.03

AK197B **Features**

High performance 32-bit RISC CPU

- Double core RISC 32-bit CPU(Support FPU)
- DC-320MHz operation
- 128 Vectored interrupts
- Four Levels interrupt priority

Image Signal Processor

- Support DVP and BT656 interface timing
- Support YUV422 format (Input)
- Support YUV422 and YUV420 format (Output)
- Support 720p@30fps input size

Flexible I/O

- 28 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

Peripheral Feature

- FUSB 1.1 OTG controller
- Audio interface supports IIS, left adjusted, right adjusted and DSP mode
- Multi-function 32-bit timers, support capture and PWM mode
- 16-bit PWM generator for motor driving
- Three full-duplex advanced UART
- Three SPI interface supports host and device mode
- Two SD Card Host controller
- One IIC interface supports host and device mode
- One SPDIF receiving interface without analog amplify
- Quadrate decoder
- Watchdog
- One Crystal Oscillator
- One channel 16-bit DAC with headphone amplifier
- Four channels Audio 16-bit ADC
- Four channels MIC amplifier
- Four channels analog MUX
- Ten channels 10-bit ADC
- Power-on reset
- Embedded PMU support low power mode

Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth V2.1(BR+EDR)+ BLE V5.3 specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Support GFSK and π/4 DQPSK all paket types
- Provides +15dbm transmitting power
- Receiver with -93dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp \att\gap\gatt\rfcomm\sdp\l2cap profile

WIFI Feature

- Support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~ MCS7, MCS32, 20MHz/40MHz BW, 800ns and 400ns guard interval.
- Support advanced 1x1 802.11n features:
  Full / Half Guard Interval
  Frame Aggregation
  Reduced Inter-frame Space (RIFS)
  Space Time Block Coding (STBC)
  Greenfield mode

- Support WEP/WPA-PSK(TKIP/CCMP) /WPA2-PSCK/AES256/AES128/SHA256 /SHA128
- Support apply to AP/STA
- Transmitter power:

  DSSS 1M/S 17 dBm
  MCS0 16 dBm
  MCS7 13 dBm
- Receiver sensitivity:

  DSSS 1M/S -95 dBm
  MCS0 -92 dBm
  MCS7 -74 dBm

Packages

- QFN48(6mm*6mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

1. Pin Definition

1.1 Pin Assignment

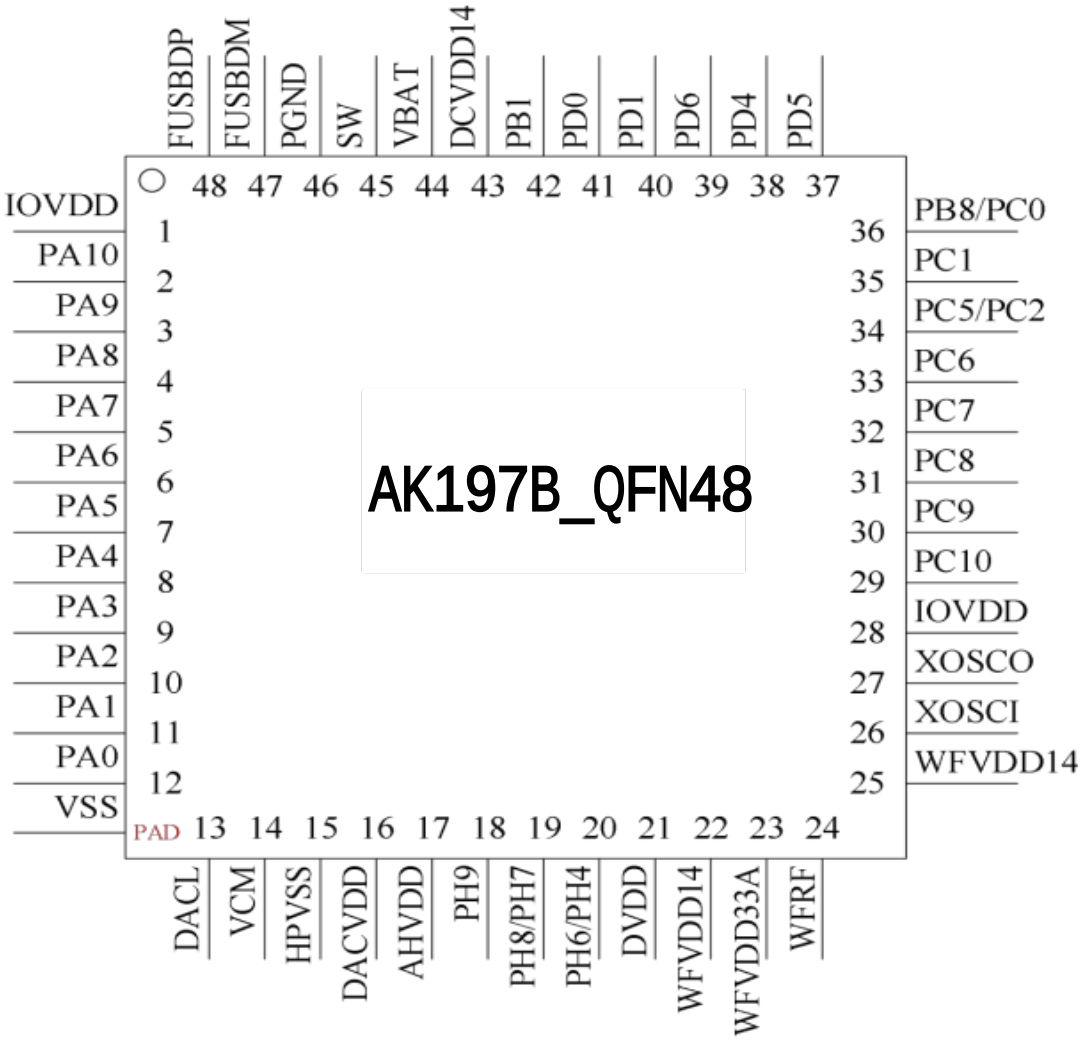


Figure 1-1 AK197B _QFN48 Package Diagram

1.2 Pin Description

Table 1-1 AK197B _QFN48 Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	IOVDD	P	/	IO Power 3.3V	-
2	PA10	I/O	24/16/8/2.4	GPIO	LCD_SYNC1_A: LCD Synchronization1(A) SENSOR0_SYNC1_A: Sensor0 Synchronization1(A) SD0_DAT1B: SD0 Data1(B) ALNK0_DAT3B1: Audio Link0 Data3(B1) ALNK1_DAT3B1: Audio Link1 Data3(B1) ADC2: ADC Channel 2 TMR7CK(MCPWM)
3	PA9	I/O	24/16/8/2.4	GPIO	LCD_SYNC0_A: LCD Synchronization0(A) SENSOR0_SYNC0_A: Sensor0 Synchronization0(A) SD0_DAT0B: SD0 Data0(B) ALNK0_DAT2B1: Audio Link0 Data2(B1) ALNK1_DAT2B1: Audio Link1 Data2(B1) TMR6CK(MCPWM)
4	PA8	I/O	24/16/8/2.4	GPIO	LCD_CLK_A: LCD Clock(A) SENSOR0_CLK_A: Sensor0 Clock(A) IIC_SDA_B: IIC SDA(B) SD0_CLKB: SD0 Clock(B) ALNK0_DAT1B1: Audio Link0 Data1(B1) ALNK1_DAT1B1: Audio Link1 Data1(B1) SPDIF_D ADC1: ADC Channel 1 PWMCH1L(MCPWM) Wakeup4: Port Wakeup 4 SDTAP_DATD
5	PA7	I/O	24/16/8/2.4	GPIO	LCD_D0_A: LCD Data0(A) SENSOR0_D7_A: Sensor0 Data7(A) IIC_SCL_B: IIC SCL(B) SD0_CMDB: SD0 CMD(B) ALNK0_DAT0B1: Audio Link0 Data0(B1) ALNK1_DAT0B1: Audio Link1 Data0(B1) SPDIF_C ADC0: ADC Channel 0 PWMCH1H(MCPWM) TMR0: Timer0 Clock In Wakeup3: Port Wakeup 3 SDTAP_CLKD

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
6	PA6	I/O	24/16/8/2.4	GPIO	LCD_D1_A: LCD Data1(A) SENSOR0_D6_A: Sensor0 Data6(A) UART0_RXA: Uart0 Data In(A) SD0_DAT3B: SD0 Data3(B) ALNK0_LRCKB1: Audio Link0 Word Select (B1) ALNK1_LRCKB1: Audio Link1 Word Select(B1) FPIN0(MCPWM)
7	PA5	I/O	24/16/8/2.4	GPIO	LCD_D2_A: LCD Data2(A) SENSOR0_D5_A: Sensor0 Data5(A) UART0_TXA: Uart0 Data Out(A) SD0_DAT2B: SD0 Data2(B) AMUX2: Simulator Channel 2 ALNK0_SCLKB1: Audio Link0 Serial Clock(B1) ALNK1_SCLKB1: Audio Link1 Serial Clock(B1) CAP3: Timer3 Capture
8	PA4	I/O	24/16/8/2.4	GPIO	LCD_D3_A: LCD Data3(A) SENSOR0_D4_A: Sensor0 Data4(A) CLKOUT1: Clock Out1 SPI2_DOC: SPI2 Data Out(C) MIC2N: MIC2 N Channel ALNK0_MCKB1: Audio Link0 Master Clock(B1) ALNK1_MCKB1: Audio Link1 Master Clock(B1) UART0_RXC: Uart0 Data In(C) PWMCH0L(MCPWM)
9	PA3	I/O	24/16/8/2.4	GPIO	LCD_D4_A: LCD Data4(A) SENSOR0_D3_A: Sensor0 Data3(A) SPI2_CLKC: SPI2 Clock(C) MIC2P: MIC2 P Channel UART0_TXC: Uart0 Data Out(C) PWMCH0H(MCPWM)
10	PA2	I/O	24/16/8/2.4	GPIO	LCD_D5_A: LCD Data5(A) SENSOR0_D2_A: Sensor0 Data2(A) SPI2_DIC: SPI2 Data In(C) MIC0P: MIC0 P Channel TMR0CK(MCPWM)
11	PA1	I/O	24/16/8/2.4	GPIO	LCD_D6_A: LCD Data6(A) SENSOR0_D1_A: Sensor0 Data1(A) MIC0N: MIC0 N Channel PWM0: Timer0 PWM Output

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
12	PA0	I/O	24/16/8/2.4	GPIO	LCD_D7_A: LCD Data7(A) SENSOR0_D0_A: Sensor0 Data0(A) AMUX0: Simulator Channel 0 TMR1CK(MCPWM) Wakeup2: Port Wakeup 2
13	DACL	O	/	DAC Left Channel	-
14	VCM	P	/	VCM	-
15	HPVSS	P	/	Audio Ground	-
16	DACVDD	P	/	DAC Power	-
17	AHVDD	P	/	Audio Power	-
18	PH9	I/O	24/16/8/2.4	GPIO	MIC1P: MIC1 P Channel
19	PH8	I/O	24/16/8/2.4	GPIO	MIC1N: MIC1 N Channel
	PH7	I/O	24/16/8/2.4	GPIO	AMUX1: Simulator Channel 1 UART1_RXA: Uart1 Data In(A) PWMCH5L(MCPWM) Wakeup13: Port Wakeup 13
20	PH6	I/O	24/16/8/2.4	GPIO	MIC3P: MIC3 P Channel UART1_TXA: Uart1 Data Out(A) FPIN3(MCPWM) PWM2: Timer2 PWM Output
	PH4	I/O	24/16/8/2.4	GPIO	AMUX3: Simulator Channel 3 FPIN4(MCPWM)
21	DVDD	P	/	Core Power 1.2V	-
22	WFVDD14	P	/	RF Power 1.4V	-
23	WFVDD33A	P	/	RF Power 3.3V	-
24	WFRF	-	/	RF Antenna	-
25	WFVDD14	P	/	RF Power 1.4V	-
26	XOSCI	I	/	RF OSCI	-
27	XOSCO	O	/	RF OSCO	-
28	IOVDD	P	/	IO Power 3.3V	-
29	PC10	I/O	24/16/8/2.4	GPIO	SD0_CLKD: SD0 Clock(D) SPI1_DOB: SPI1 Data Out(B) ISP_DI_B Q-decoder1 UART2_RXB: Uart2 Data In(B) ADC9: ADC Channel 9 TMR5CK(MCPWM) PWM3: Timer3 PWM Output TOUCH10: Touch Input Channel 10 SDTAP_DATA

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
30	PC9	I/O	24/16/8/2.4	GPIO	SD0_CMDD: SD0 CMD(D) SPI1_CLKB: SPI1 Clock(B) ISP_CLK_B Q-decoder0 UART2_TXB: Uart2 Data Out(B) ADC8: ADC Channel 8 TMR4CK(MCPWM) TOUCH9: Touch Input Channel 9 SDTAP_CLKA
31	PC8	I/O	24/16/8/2.4	GPIO	SD0_DAT0D: SD0 Data0(D) SPI1_DIB: SPI1 Data In(B) SPDIF_B PWMCH2L(MCPWM) CAP5: Timer5 Capture TOUCH8: Touch Input Channel 8
32	PC7	I/O	24/16/8/2.4	GPIO	SD0_DAT1D: SD0 Data1(D) SPDIF_A PWMCH2H(MCPWM) CAP4: Timer4 Capture TOUCH7: Touch Input Channel 7
33	PC6	I/O	24/16/8/2.4	GPIO	SD0_DAT2D: SD0 Data2(D) ALNK0_DAT3A: Audio Link0 Data3(A) ALNK1_DAT3A: Audio Link1 Data3(A) TMR3CK(MCPWM) PWM5: Timer5 PWM Output TOUCH6: Touch Input Channel 6
34	PC5	I/O	24/16/8/2.4	GPIO	SD0_DAT3D: SD0 Data3(D) ALNK0_DAT2A: Audio Link0 Data2(A) ALNK1_DAT2A: Audio Link1 Data2(A) TMR2CK(MCPWM) PWM4: Timer4 PWM Output TOUCH5: Touch Input Channel 5
	PC2	I/O	24/16/8/2.4	GPIO	IIC_SDA_C: IIC SDA(C) ALNK0_LRCKA: Audio Link0 Word Select(A) ALNK1_LRCKA: Audio Link1 Word Select(A) SD1_DAT0B: SD1 Data0(B) PWMCH4L(MCPWM) CAP1: Timer1 Capture TOUCH2: Touch Input Channel 2

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
35	PC1	I/O	24/16/8/2.4	GPIO	IIC_SCL_C: IIC SCL(C) ALNK0_SCLKA: Audio Link0 Serial Clock(A) ALNK1_SCLKA: Audio Link1 Serial Clock(A) SD1_CLKB: SD1 Clock(B) ADC7: ADC Channel 7 PWM1: Timer1 PWM Output Wakeup11: Port Wakeup 11 TOUCH1: Touch Input Channel 1
36	PC0	I/O	24/16/8/2.4	GPIO	CLKOUT0: Clock Out0 ALNK0_MCKA: Audio Link0 Master Clock(A) ALNK1_MCKA: Audio Link1 Master Clock(A) SD1_CMDB: SD1 CMD(B) ADC6: ADC Channel 6 PWMCH4H(MCPWM) Wakeup10: Port Wakeup 10 TOUCH0: Touch Input Channel 0
	PB8	I/O	24/16/8/2.4	GPIO	SDGAT: SD Power Gate
37	PD5	I/O	24/16/8/2.4	GPIO	SPI0_DOA(0): SPI0 Data Out(A) SFC_DOA(0): SFC Data Out(A)
38	PD4	I/O	24/16/8/2.4	GPIO	SPI0_CLKA: SPI0 Clock(A) SFC_CLKA: SFC Clock(A)
39	PD6	I/O	24/16/8/2.4	GPIO	SFGAT: Flash Power Gate
40	PD1	I/O	24/16/8/2.4	GPIO	SPI0_DIA(1): SPI0 Data In(A) SFC_DIA(1): SFC Data In(A)
41	PD0	I/O	24/16/8/2.4	GPIO (pull up)	SPI0_CSA: SPI0 Chip Select(A) SFC_CSA: SFC Chip Select(A)
42	PB1	I/O	24/16/8/2.4	GPIO (pull up)	ISP_DO UART0_TXB: Uart0 Data Out(B) ADC3: ADC Channel 3 Long Press reset TMR1: Timer1 Clock In Wakeup8: Port Wakeup 8
43	DCVDD14	P	/	Core Power 1.4V	-
44	VBAT	P	/	LDO Power	-
45	SW	P	/	DC-DC Switch Pin	-
46	PGND	P	/	PMU Ground	-

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
47	FUSBDM	I/O	10	USB Negative Data (pull down)	UART1_RXD: Uart1 Data In(D) ISP_DI_A SPI2_DOB: SPI2 Data Out(B) IIC_SDA_A: IIC SDA(A) ADC12: ADC Channel 12 SDTAP_DATB
48	FUSBDP	I/O	10	USB Positive Data (pull down)	UART1_TXD: Uart1 Data Out(D) ISP_CLK_A SPI2_CLKB: SPI2 Clock(B) IIC_SCL_A: IIC SCL(A) ADC13: ADC Channel 13 SDTAP_CLKB
PAD		P	/	VSS	-

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	5.5	V
WFVDD33A	RF Power 3.3V Voltage	-0.3	3.5	V
AHVDD	Audio Power Voltage	-0.3	3.5	V
WFVDD14	RF Power 1.4V Voltage	-0.3	1.55	V
$V_{3.3IO}$	3.3V IO Input Voltage	-0.3	IOVDD+0.3	V

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	5.5	V	_
IOVDD	Voltage output	2.1	3.3	3.5	V	LDO5V = 5V, 200mA loading
DCVDD14	Voltage output	1.2	1.4	1.55	V	LDO mode: 70mA loading DC-DC mode: 120mA loading
DVDD	Voltage output	0.87	1.2	1.32	V	LDO5V=5V, 100mA loading
WFVDD33A	Voltage Input	2.1	3.3	3.5	V	_
AHVDD	Voltage Input	2.1	3.3	3.5	V	_
WFVDD14	Voltage Input	1.2	1.4	1.55	V	_

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.3V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	–	IOVDD+0.3	V	IOVDD = 3.3V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	–	–	0.33	V	IOVDD = 3.3V
V_{OH}	High-Level Output Voltage	2.7	–	–	V	IOVDD = 3.3V

2.4 Internal Resistor Characteristics

Table 2-4

Port	**General Output**	**High Drive**	**Internal Pull-Up Resistor**	**Internal Pull-Down Resistor**	**Comment**
PA,PC,PD, PH,PB1,PB8	8mA	24mA	10K	10K	1.PB1&PD0 default pull up 2.FUSBDM & FUSBDP default pull down 3. Internal pull-up/pull-down resistance | accuracy ±20%
FUSBDP FUSBDM	10mA	–	1.5K	15K	

2.5 DAC Characteristics

Table 2-5

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	_	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	_	-72	_	dB	
S/N	_	99	_	dB	
Output Swing	_	0.9	_	Vrms	
Dynamic Range	_	93	_	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	15	_	_	mW	32ohm loading

2.6 ADC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	_	87	_	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
S/N	_	90	_	dB	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	_	-72	_	dB	
Crosstalk	_	-80	_	dB	

2.7 ESD Protection

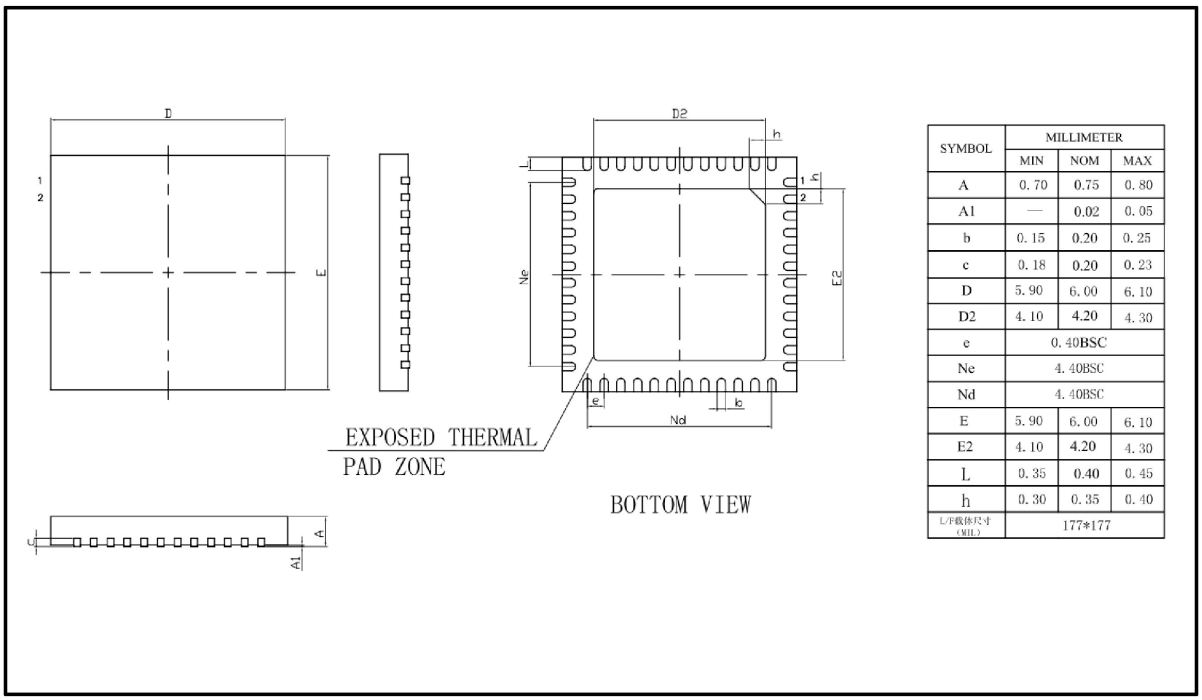
Table 2-7

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins(except WFRF)	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

3. Package Information

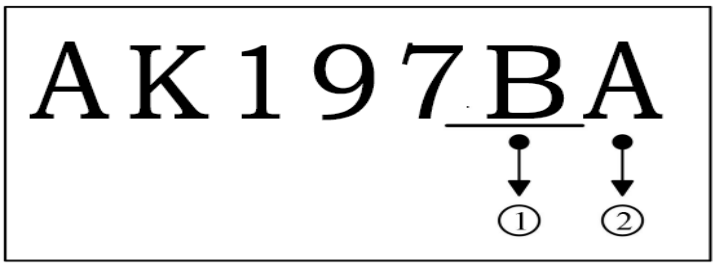
3.1 QFN48(6mm*6mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	177*177		

Figure 3-1 AK197B _QFN48 Package

4. Package Type Specification



①Represents different chips (different packages or bindings)

②Represents different memory sizes

0: No memory
2: 2Mbit Flash
4: 4Mbit Flash
8: 8Mbit Flash
6: 16Mbit Flash
3: 32Mbit Flash
5: 64Mbit Flash
7: 128Mbit Flash
A: 1Mx16 SDRAM
B: 4Mx16 SDRAM
C: 16M bit PSRAM
D: 64M bit PSRAM

5. Solder-Reflow Condition

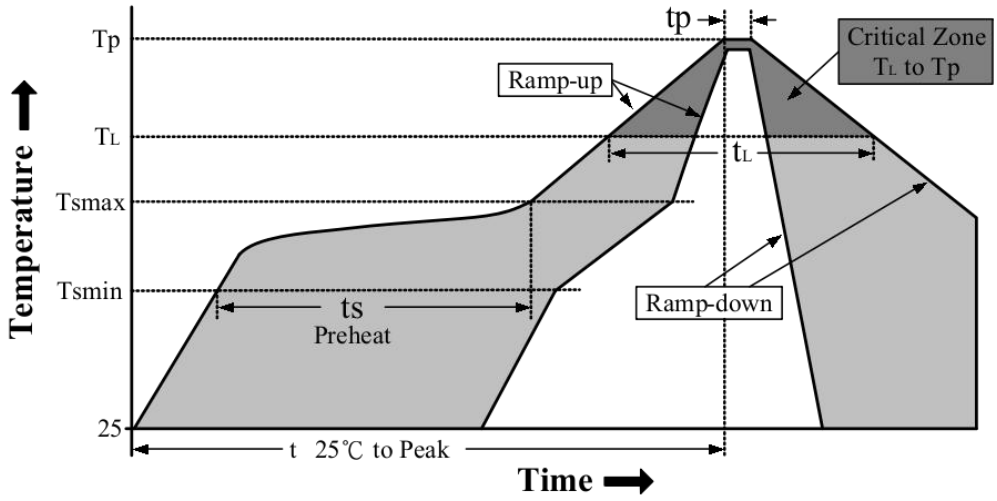


Figure 5-1 Classification Reflow Profile

Classification Profiles **Table 5-1**

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak	Temperature Min (T_{smin})	100°C	150°C
	Temperature Max (T_{smax})	150°C	200°C
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3°C/second max	3°C/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183°C 60-150 seconds	217°C 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2	See Table 6-3
Time within 5°C of actual Peak Temperature (tp)[2]		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6°C/second max	6°C/second max
Time 25°C to peak temperature		6 minutes max	8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5℃of actual peak temperature (tp) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature **Table 5-2**

Package Thickness	Volume mm^3 < 350	Volume mm^3 ⩾350
<2.5 mm	240 +0/-5℃	225 +0/-5℃
⩾2.5 mm	225 +0/-5℃	225 +0/-5℃

Pb-free - Classification Temperature **Table 5-3**

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260℃	260℃	260℃
1.6 mm - 2.5mm	260℃	250℃	245℃
> 2.5mm	250℃	245℃	245℃

6. Revision History

Date	Revision	Description
2021.08.27	V1.0	Initial Release
2021.09.03	V1.1	Modify the description of the DAC function
2022.07.20	V1.2	Updated parameter
2023.03.03	V1.3	Modify the chip feature description